ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABUS

Effective from the Academic Year 2020-21 onwards

M. Tech. Two Year Degree Course

(MR20 Regulations)

in

VLSI and Embedded Systems

Department of Electronics and Communication Engineering

MALLA REDDY ENGINEERING COLLEGE (Autonomous)

(An UGC Autonomous Institution, Approved by AICTE and Affiliated to JNTUH Hyderabad,
Recognized under 2(f) &12 (B) of UGC Act 1956, Accredited by NAAC with 'A' Grade (II Cycle)
Maisammaguda, Dhulapally (Post Via Kompally), Secunderabad-500 100
www.mrec.ac.in E-mail: principal@mrec.ac.in

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

MR18 ACADEMIC REGULATIONS (CBCS)
For M. Tech. (REGULAR) DEGREE PROGRAMME

Applicable for the students of M. Tech. (Regular) programme admitted from the Academic Year ***2018-19*** and onwards.

The M. Tech. Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the programme and who fulfill all the requirements for the award of the Degree.

INSTITUTION VISION

A Culture of excellence , the hallmark of MREC as world class education center to impart Technical Knowledge in an ambience of humanity, wisdom, intellect, creativity with ground breaking discovery, in order to nurture the students to become Globally competent committed professionals with high discipline, compassion and ethical values.

INSTITUTION MISSION

Commitment to progress in mining new knowledge by adopting cutting edge technology to promote academic growth by offering state of art Under graduate and Post graduate programmes based on well-versed perceptions of Global areas of specialization to serve the Nation with Advanced Technical knowledge.

DEPARTMENT VISION

To produce innovative, globally competent and ethical Electronics and communication Engineers to cater socio-economic needs.

DEPARTMENT MISSION

- To impart quality education in Electronics and Communication Engineering discipline and produce employable graduates
- To improve the thought process of students by exposing them to advanced technologies and make them innovative in their career
- To provide ethical and value-based education by encouraging activities addressing the societal needs.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO 1: Graduates are capable to meet the industrial expectations, have a better career and pursue higher studies in the area of machine design.

PEO 2: Graduates are encouraged to predict the technical challenges and provide optimal ways to solve through research methodologies for societal benefits.

PEO 3: Graduates are able to explore their skills to invent, design and realize new technology through lateral thinking.

PEO 4: Graduates are proficient to express their ability to work as team and lead to accomplish the professional and organizational goals with ethical and moral values.

PEO 5: Graduates keep themselves abreast of emerging technologies, continually learn new skills to nourish ever-developing careers.

PROGRAMMEOUTCOMES(POs)

PO 1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO 2: An ability to write and present a substantial technical report/document.

PO 3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO 4: Ability to develop innovative thinking in solving Engineering problems.

PO 5: Engage in Life-long learning independently with a high level of passion and profession.

PO 6: Apply contextual Knowledge to axis societal, safety legal issues, relevant to professional Engineering.

1.0 **Post-Graduate Degree Programmes in Engineering & Technology (PGP in E&T) Malla Reddy Engineering College (Autonomous) (MREC-A)** offers **Two** Year (**Four** Semesters) full-time **Master of Technology (M. Tech.)** Post Graduate programmes, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

2.0 Eligibility for Admissions:

2.1 Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the Affiliating University from time to time. Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the Government of Telangana or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.2 The medium of instructions for all PG Programmes will be **ENGLISH** only.

3.0 M.Tech. Programme (PGP in E&T) Structure and Award of Degree:

3.1 The M.Tech. Programmes in E & T are of Semester pattern, with **Four** Semesters consisting of **Two** academic years, each academic year having **Two** Semesters (First/ Odd and Second/ Even Semesters). Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per Semester.

3.2 A student shall be declared eligible for the award of the M.Tech. Degree, if the student pursues a course of study in not less than two and not more than four academic years. However, the student is permitted to write the examinations for two more years after four academic years of course work, failing which the student shall forfeit the seat in M. Tech. programme.

3.3 The student shall register for all **68** credits and secure all the **68** credits.

3.4 **UGC/ AICTE** specified definitions/ descriptions are adopted appropriately for various terms
and Abbreviations used in these PG academic regulations, as listed below:

3.4.1 Semester Scheme

Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' and 'COURSE' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Design/ Drawing Subject', or 'Seminar', or 'Project', or "Technical Paper Writing" as the case may be.

3.4.2 Credit Courses

All subjects/courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/course in an L: T: P: C (Lecture Periods: Tutorial Periods: Practical Periods: Credits) structure based on the following general pattern:

- One credit for one hour/week/semester for theory/lecture (L) / tutorials (T) courses
- One credit for two hours/ week/semester for laboratory/ practical (P) courses

Other student activities like study tour, guest lecture, conference/workshop participations, technical paper presentations, and identified mandatory/audit courses, if any, will not carry credits.

3.4.3 Subject / Course Classification

All subjects / courses offered for the Post-Graduate Programme in E & T (M.Tech Degree Programme) are broadly classified as follows. The Institution has followed in general, the guidelines issued by AICTE/UGC.

S.No	Broad Course Classification	Course Group/ Category	Course Description
1	Core Courses (CC)	PC- Professional Core	Includes subjects related to the parent discipline/ department/ branch of Engineering
		Project Work	M.Tech Project / Dissertation
		Seminar	Seminar/ Colloquium based on core contents related to parent discipline/ department/ branch of Engineering
2	Elective Courses (EC)	PE - Professional Electives	Includes elective subjects related to the parent discipline/ department/ branch of Engineering
		OE - Open Electives	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline/ department/ branch of Engineering
3	Audit Courses (AC)	Audit Courses	These courses are non-credit courses without evaluation.
Total Number of Credits – 68 credits			

3.4.4 Courses of Study:

The following specializations are offered at present for the M. Tech. programme of study.

S.No.	Dept.	Specialization Code	Specialization	Intake
1	CE	11	Structural Engineering (SE)	24
2	EEE	24	Electrical Power Systems (EPS)	24
3	ME	31	Thermal Engineering (TE)	18
4		33	Machine Design (MD)	24
5	CSE	51	Computer Science and Engineering (CSE)	18

Any other programme as approved by the University from time to time.

4 Course Registration:

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice/ Option for Subjects/ Courses, based on his competence, progress, pre-requisites and

interest.

4.2 The Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work for the first semester through 'ON-LINE SUBMISSIONS', ensuring 'DATE and TIME Stamping'. The ON-LINE Registration Requests for any 'SUBSEQUENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'CURRENT SEMESTER'.

4.3 A Student can apply for ON-LINE Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from the Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries during ON-LINE Registration for the Subject(s) / Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Subject/ Course in that Category will be taken into consideration.

4.5 Subject/ Course Options exercised through ON-LINE Registration are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Subject/ Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new Subject (subject to offering of such a Subject), or for another existing Subject (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5 Attendance Requirements:

The programmes are offered on a module basis with each subject/course being considered as a module.

5.1 Attendance in all classes (Theory/Laboratories/Seminar/Project Work) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the attendance of mid-term examination / Laboratory and the days of attendance in sports, games, NCC and NSS activities for appearing for the Semester End Examination (SEE). A student shall not be permitted to appear for the Semester End Examinations (SEE) if his attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee (CAC).

5.3 Shortage of Attendance below 65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their Semester End Examination of that subject and their registration shall stand cancelled.

5.5 A stipulated fee prescribed by the CAC, shall be payable towards Condonation for shortage of attendance.

5.6 A candidate shall put in a minimum required attendance in at least three (3) theory subjects in I Year I semester for promoting to I Year II Semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic

requirements of the subjects, as per the course structure.

5.7 A student shall not be promoted to the next semester unless the student satisfies the attendance requirement of the present Semester, as applicable. The student may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, the student shall not be eligible for readmission into the same class.

6 Academic Requirements:

The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item 5.

6.1 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the Semester End Examination and a minimum of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together. In case the candidate does not secure the minimum academic requirement in any subject he has to reappear for the Semester End Examination in that subject. A candidate shall be given one chance to re-register for the subject if the internal marks secured by the candidate are less than 50% and failed in that subject. This is allowed for a maximum of three subjects and should register within two weeks of commencement of that semester class work. In such a case, the candidate must re-register for the subjects and secure the required minimum attendance. The candidate's attendance in the re-registered subject(s) shall be calculated separately to decide upon the eligibility for writing the Semester End Examination in those subjects. In the event of the student taking another chance, the student's Continuous Internal Evaluation (CIE) marks and Semester End Examination (SEE) marks obtained in the previous attempt stands cancelled.

6.2 If the student secured 'F' grade in any subject he/she can apply for recounting / revaluation by paying prescribed fee. If the student is not satisfied after the results declaration of recounting / revaluation he/she can apply for challenge valuation with the prescribed fee. College appoints a faculty member; student can bring another faculty member who taught the respective subject at least once (proof should be provided). The faculty member should be from any autonomous college affiliated to JNTUH or JNTUH constituent colleges.

7 Evaluation - Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned) for 100 marks for Theory, Practicals, Seminar, Drawing / Design, Project, and Minor Courses etc.,. The Theory / Practical courses are evaluated with two components. 1. Continuous Internal Evaluation (CIE), 2. Semester End Examination (SEE). The distribution shall be 30 marks for CIE and 70 marks for SEE decided in the Academic Council.

7.1 Theory Courses :

7.1.1 Continuous Internal Evaluation (CIE):

CIE shall be conducted for all courses of PG Programmes twice in a semester (2 Midterm examinations) with the help of objective, subjective evaluation and regular assignments. Each midterm examination consists of objective, subjective paper and one assignment. The

objective and subjective test shall be evaluated to 40 % and 50 % for duration of 120 mins and the assignment evaluated for 10 % of the allocated internal marks.

The division of marks for CIE is as given below:

Mid – Term Examination				
Part	**Type of Questions**	**No. of questions**	**Marks per question**	**Total**
Part A	Multiple-choice questions	10	1	10
	Fill-in the blanks	10	1	10
	Sub-Total			20
Part B	Compulsory questions [With Module-wise internal choice]	5	5	25
			Mid-Term Exam Total	45
			Assignment	05
			Grand Total	50

*The CIE will be conducted for 50 marks and scaled to 30 marks.

The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus. First Assignment should be submitted before the conduct of the first mid-term examinations, and the Second Assignment should be submitted before the conduct of the second midterm examinations. The weightage for the midterm examination shall be given as 70% of the best performing midterm examination and 30% of the other performing midterm examination. The student shall appear for both midterm examinations. In case for any specific reason the student appears only for one midterm examination, only 70% weightage of that examination shall be considered.

7.1.2 Semester End Examination (SEE):

Semester End Examination (SEE) shall be conducted for all courses of PG Programmes at the end of the Semester. Duration of the examination is 3 hours. The paper setting and evaluation of all courses carried out by external examiners. The examiners will be selected by the chief controller of examination/ Principal.

Type of Questions	No. of Questions	Marks per Question	Total
Essay Type Answer Questions [For each question there will be an 'either or choice', which means that there will be two questions from each module and the student should answer either of the two questions.]	5	14	70

7.2 Practical Courses:

7.2.1 Continuous Internal Evaluation (CIE):

CIE marks shall be awarded with a distribution of 40% for day - to-day performance

and timely submission of lab records, 40% for internal lab exam (best out of two exams) and 20% for viva-voce. The CIE will be conducted for 50 marks and scaled to 30 marks.

7.2.2 Semester End Examination (SEE):

SEE marks shall be awarded with a distribution of 20% for design/procedure/schematic diagram of the given experiment, 40% for conduction of experiment, 20% for results and 20% for viva - voce. For conducting SEE (with duration of 3 hours), one internal examiner and one external examiner will be appointed by the Chief Controller of Examinations/Principal of the college. The external examiner should be selected from outside the college among the autonomous / reputed institutions from a panel of three examiners submitted by the concerned Head of the Department.

7.3 Seminar:

There shall be a seminar presentation during III semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Department PG Coordinator, Supervisor and two other senior faculty members of the department. For Seminar there will be only internal evaluation. Out of the total allocated marks distribution of marks shall be 30% for the report, 50% for presentation and 20% for the queries. A candidate has to secure a minimum of 50% of marks to be declared successful. If the student fails to fulfill minimum marks, the student has to reappear during the supplementary examinations. There shall be no semester end examinations for the seminar.

7.4 Evaluation of Project/ Dissertation Work :

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

7.4.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson/Department PG Coordinator, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

7.4.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

7.4.3 After satisfying 7.4.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and action plan of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

7.4.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

7.4.5 A candidate shall submit his project status report in two stages at least with a gap of 2

months between them.

7.4.6 The work on the project shall be initiated at the beginning of the III Semester and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.
Note: *The project supervisor/guide has to ensure that the student has to publish a minimum of one paper based on his/her thesis in an International Journal of repute preferably in UGC CARE-Group I list*.

7.4.7 For the final approval by the PRC, the soft copy of the thesis should be submitted for ANTI-PLAGIARISM check for the quality and the plagiarism report should be included in the final thesis. If the similarity information is less than 24%, then only thesis will be accepted for submission.

7.4.8 Three copies of the Project Thesis certified by the supervisor, HOD shall be submitted to the Chief Controller of Examinations /Principal for project evaluation (Viva Voce).

7.4.9 For Project/Dissertation phase-I in III Semester is internal evaluation only. The evaluation marks shall be carried out with a distribution of 70% evaluated by the PRC and 30% by Supervisor. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work and Literature Survey in the same domain. A candidate has to secure a minimum of 50% of the allocated marks to be declared successful for Project work Part-I. If the student fails to fulfill minimum marks, the student has to reappear during the supplementary examination.

7.4.10 For Project/Dissertation phase-II in IV Semester is an external evaluation. The evaluation shall be carried out by the External examiner appointed by the Chief Controller of Examinations/Principal. For this, the Head of the Department shall submit a panel of 3 examiners, eminent in that field, with the help of the supervisor/guide concerned. The distribution of marks followed by Quality of the work (Plagiarism), Paper publication, nature of the work (Tools & software used and Innovative ideas), presentation and Viva-Voce - each for 20% of allocated marks. The candidate has to secure minimum of 50% marks in Project Evaluation (Viva-Voce) examination.

7.4.11 If the student fails to fulfill as specified in 7.4.10, based on the recommendation of the external examiner, the student will reappear for the Viva-Voce examination with the revised thesis only after three months. In the reappeared examination also, fails to fulfill, the student will not be eligible for the award of the degree.

7.4.12 The Head of the Department shall coordinate and make necessary arrangements for the conduct of Project Viva-Voce examination.

7.5 Non-Credit Courses:

7.5.1 Audit Courses:

Audit Courses offered in any Semester, a '**Satisfactory Participation Certificate**' shall be issued to the student from the concerned authorities, only after securing $\geq$ 65% attendance in such a course. No marks or Letter Grade shall be allotted for these activities.

8 Examinations and Assessment - The Grading System:

8.1 Grades will be awarded to indicate the performance of each student in each Theory Subject, or Lab / Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 6 above, and a corresponding Letter Grade shall be given.

8.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	**Grade Points**	**Letter Grade (UGC Guidelines)**
≥ 90%,	10	O (Outstanding)
(≥ 80%, <90%)	9	A+ (Excellent)
(≥ 70%, < 80%)	8	A (Very Good)
(≥ 60%, < 70%)	7	B+ (Good)
(≥ 55%, < 60%)	6	B (Average)
(≥ 50%, < 55%)	5	C (Pass)
(< 50%)	0	F(Fail)
Absent	0	Ab

8.3 A student obtaining F Grade in any Subject shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when conducted. In such cases, his Internal Marks (CIE Marks) in those Subjects will remain the same as those he obtained earlier.

8.4 A student not appeared for examination then 'Ab' Grade will be allocated in any Subject shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when conducted.

8.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

8.6 In general, a student shall not be permitted to repeat any Subject/ Course (s) only for the sake of 'Grade Improvement' or 'SGPA/ CGPA Improvement'.

8.7 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course. The corresponding 'Credit Points' (CP) is computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

8.8 The Student passes the Subject/ Course only when he gets GP ≥ 5(C Grade or above).

8.9 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (∑CP) secured from ALL Subjects/ Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as:

$$\mathbf{SGPA} = \left\{\sum_{i=1}^{N} C_i G_i\right\} / \left\{\sum_{i=1}^{N} C_i\right\} \ldots \textbf{ For each Semester}$$

where 'i' is the Subject indicator index (takes into account all Subjects in a Semester), 'N'is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to the i^{th} Subject, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that i^{th} Subject.

8.10 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the II Semester onwards, at the end of each Semester, as per the formula:

$$\mathbf{CGPA} = \left\{\sum_{j=1}^{M} C_j G_j\right\} / \left\{\sum_{j=1}^{M} C_j\right\} \textbf{ … for all S semesters registered}$$

(i.e., upto and inclusive of S semesters, S ≥ 2)

where 'M' is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1stSemester onwards upto and inclusive of the Semester S (obviously M > N), 'j' is the Subject indicator index (takes into account all Subjects from 1 to S Semesters), C_j is the no. of Credits allotted to the j^{th} Subject, and G_j represents the Grade Points (GP)corresponding to the Letter Grade awarded for that j^{th} Subject. After registration and completion of I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA

Course/Subject	Credits	Letter Grade	Grade Points	Credit Points
Course 1	3	A	8	3X8=24
Course 2	3	O	10	3X10=30
Course 3	3	B	6	3X6=18
Course 4	3	A+	9	3X9=27
Course 5	2	B+	7	2X7=14
Course 6	2	A	8	2X8=16
Course 7	2	B	6	2X6=12
	18			141
SGPA = 141/18 = 7.83				

Illustration of calculation of CGPA

Semester	Credits	SGPA	Credits X SGPA
Semester I	18	7	18 X 7 = 126
Semester II	18	6	18 X 6 = 108
Semester III	16	6.5	16 X 6.5 = 104
Semester IV	16	7.25	16 X 7.25 = 116
	68		454
CGPA = 454/68 = 6.67			

8.11 For Calculations listed in Item 8.6 – 8.10, performance in failed Subjects/ Courses (securing 'F' Grade) will also be taken into account, and the Credits of such Subjects/Courses will also be included in the multiplications and summations.

9. Award of Degree and Class:

9.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of **68** Credits (with CGPA $\geq$ 5.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

9.2 Award of Class

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 8.00
First Class	≥ 6.50 and < 8.00
Second Class	≥ 5.00 and < 6.50

9.3 A student with final CGPA (at the end of the PGP) < 5.00 will not be eligible for the Award of Degree.

9.4 Students will be eligible for the award of **'Gold Medal'** , if he/she passes all the subjects / courses in first appearance within the first academic years (or four sequential semesters) from the date of commencement of first year first semester and should have secure CGPA ≥ 8.00 at the end of four sequential semesters.

10 Withholding of Results:

If the student has not paid the dues, if any, to the Institution/University or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

11 Transitory Regulations:

11.1 If any candidate is detained due to shortage of attendance in one or more subjects, they are eligible for re-registration to maximum of two earlier or equivalent subjects at a time as and when offered.

11.2 The candidate who fails in any subject will be given two chances to pass the same subject;
otherwise, he has to identify an equivalent subject as per MR18 Academic Regulations.

12. Student Transfers:

12.1 There shall be no Branch/Specialization transfers after the completion of Admission Process.

12.2 The students seeking transfer to MALLA REDDY ENGINEERING COLLEGE (Autonomous)- MREC(A) from various other Universities/ institutions have to pass the failed subjects which are equivalent to the subjects of MREC(A), and also pass the subjects of MREC(A) which the students have not studied at the earlier institution. Further, though the students have passed some of the subjects at the earlier institutions, if the same subjects are prescribed in different semesters of MREC (A), the students have to study those subjects in MREC (A) in spite of the fact that those subjects are repeated.

12.3 The transfer students from other Universities / Institutions to MREC (A) who are on rolls will be provided one chance to write internal examinations in the failed subjects and/or subjects not studied as per the clearance letter issued by the JNTUH.

13. General:

13.1 **Credit**: A module by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

13.2 **Credit Point:** It is the product of grade point and number of credits for a course.

13.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they shall include “she”, “her” also.

13.4 The academic regulation should be read as a whole for the purpose of any interpretation.

13.5 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the College Academic Committee headed by the Principal is final.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR IMPROPER CONDUCT IN EXAMINATIONS

Sl.No.	Nature of Malpractices/ Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the SEE)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to that course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester. The Hall Ticket of the candidate shall be cancelled.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester. The

		candidate is also debarred for two consecutive semesters from class work and all SEE. The continuation of the programme by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all SEE. The continuation of the programme by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course.
6	Refuses to obey the orders of the Chief Controller of Examinations (CCE) / Controller of Examinations (CE)/ Assistant Controller of Examinations (ACE) / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police cases registered against them.

	act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination	
7	Leaves the exam hall taking away answer scriptor intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all SEE. The continuation of the programme by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already

		appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that course and all other courses the candidate has appeared including practical examinations and project work of that SEE.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the CCE for further action toward suitable punishment.	

Note: ***The student(s) found indulging in malpractices during the CIE also will be punished based on the recommendations of the College Academic Committee.***

Malpractices identified by squad or special invigilators

1. Punishments to the students as per the above guidelines.

MALLA REDDY ENGINEERING COLLEGE (Autonomous)

ELECTRONICS AND COMMUNICATION ENGINEERING (ECE)

Proposed Course Structure for PG - M.Tech. (VLSI & Embedded Systems) Programme

I YEAR I SEMESTER

S. No	Category	Course Code	Name of the Course	Contact Hours/Week			Credits
				L	T	P	
1	PCC	A4101	CMOS Analog IC Design	3	-	-	3
2	PCC	A4102	Embedded System Design	3	-	-	3
3	PCC	A4103	CMOS Mixed Signal Circuit Design	3	-	-	3
4	PEC-I	A4110	VLSI Design and Technology	3	-	-	3
		A4111	Advance Digital System Design				
		A4112	Algorithms for VLSI Design Automation				
5	PEC-II	A4113	Embedded Real Time Operating Systems	3	-	-	3
		A4114	Embedded Programming				
		A4115	Digital Signal Processors and Architectures				
6	PCC	A4104	Mixed Signal Design Lab	-	-	4	2
7	PCC	A4105	Embedded System Design Lab	-	-	4	2
8	AC	A0A04	English for Research Paper Writing	2	-	-	-
Total				**17**	**-**	**8**	**19**
Contact Hours: 25							

I YEAR II SEMESTER

S. No	Category	Course Code	Name of the Course	Contact Hours/Week			Credits
				L	T	P	
1	PCC	A4106	CMOS Digital IC Design	3	-	-	3
2	PCC	A4107	Advanced Embedded Processors	3	-	-	3
3	PEC-III	A4116	Design of Fault Tolerant Systems	3	-	-	3
		A4117	Low Power VLSI Design				
		A4118	CPLD and FPGA Architecture and Applications				
4	PEC-IV	A4119	Hardware and Software Co-Design	3	-	-	3
		A4120	Embedded Network Controllers				
		A4121	System On-Chip Architecture				
5	HSMC	A0H11	Research Methodology and IPR	2	-	-	2
6	PCC	A4108	Digital IC Design Lab	-	-	4	2
7	PCC	A4109	Advanced Embedded Systems Lab	-	-	4	2
8	AC	A0A05	Value Education	2	-	-	-
Total				**16**	**-**	**8**	**18**
Contact Hours: 24							

II YEAR I SEMESTER

S. No	Category	Course Code	Name of the course	Contact hours/week			Credits
				L	T	P	
1	PEC-V	A4122	Image & Video Processing	3	-	-	3
		A4123	Sensors and Actuators				
		A4124	Wireless Sensor Networks				
2	OEC		Open Elective	3	-	-	3
3	PROJ	A41P1	Technical Seminar	-	-	2	1
4	PROJ	A41P2	Project / Dissertation Phase - I	-	-	16	8
Total				**6**	**-**	**18**	**15**
Contact Hours: 24							

II YEAR II SEMESTER

S. No	Category	Course Code	Name of the course	Contact hours/week			Credits
				L	T	P	
1	PROJ	A41P3	Project / Dissertation Phase - II	-	-	32	16
Total				**-**	**-**	**32**	**16**
Contact Hours: 32							

- PCC - Professional Core Course
- PEC - Professional Elective Course
- OEC - Open Elective Course
- PROJ - Project

LIST OF OPEN ELECTIVE COURSES

S. No	Category	Course Code	Name of the course	Contact hours/week			Credits
				L	T	P	
1	OEC	A5128	Business Analytics	3	-	-	3
		A0B20	Advance Optimization Technique				
		A3228	Industrial Safety				
		A0522	Internet of Things				
		A0623	Artificial Intelligence				

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4101	CMOS ANALOG IC DESIGN	L	T	P
Credits: 3		3	-	-

PREREQUISITES: CMOS and VLSI Technology.

OBJECTIVE: To learn about MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modelling - Simple MOS Large-Signal Model, Small-Signal Model for the MOS Transistor, to learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp, to know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open- Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators

Module - I: MOS DEVICES AND MODELING [9 Periods]
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model forth MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

Module -II: ANALOG CMOS SUB-CIRCUITS [9 Periods]
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascade current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

Module -III: CMOS AMPLIFIERS [8 Periods]
Inverters, Differential Amplifiers, Cascade Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

Module -IV: CMOS OPERATIONAL AMPLIFIERS [9 Periods]
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

Module -V: COMPARATORS [9 Periods]
Characterization of Comparator, Two-Stage, Open-Loop Comparators, other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:
1. Philip E. Allen and Douglas R. Holberg, **CMOS Analog Circuit Design,**

Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, **Analysis and Design of Analog Integrated Circuits**, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. David A. Johns, Ken Martin, **Analog Integrated Circuit Design,** Wiley Student Edn, 2013.
2. Behzad Razavi, **Design of Analog CMOS Integrated Circuits**, TMH Edition.
3. Baker, Li and Boyce, **CMOS: Circuit Design, Layout and Simulation,** PHI.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Learn about MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Small- Signal Model for the MOS Transistor.
2. Learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two- Stage Op Amps, and Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, and Measurement Techniques of OP Amp.
3. Know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4102	EMBEDDED SYSTEM DESIGN	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Digital Electronics and Microprocessors.

OBJECTIVE: This course introduces the fundamental concepts of Micro Controllers and their architecture. To enable the students to write efficient programs in assembly language programs and to make the students aware of the interfacing techniques so that they can design and develop a microcontroller-based system. It also includes the embedded systems building blocks.

MODULE - I: **8051 Architecture** [**10 Periods]**

Introduction to micro controllers, comparing micro processors and micro controllers 4,8,16 and 32 bit micro controllers, Development systems for Micro controllers, Architecture; Architecture of 8051, pin configuration of 8051 micro controller, hardware input pins, output pins ports and external memory, counters and timers, serial data input and output and interrupts.

MODULE - II: **8051 Instructions** **[14 Periods]**

Addressing modes, External Data moves, Code Memory Read-only Data Moves, PUSH and POP OP codes, Data Exchanges, Logical Operations; Byte-Level Logical Operations, Bit Level Logical Operations, Rotate and Swap Operations. Flags, Incrementing and Decrementing, Addition, Subtraction, Multiplication and Division, Decimal Arithmetic, Jump and Call op codes; The jump and call program range, Jumps, Calls and Subroutines, call and returns, Interrupts and Returns.

MODULE - III: **8051 Interfacing** **[16 Periods]**

8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing and DC motor interfacing and programming.

MODULE - IV: **Introduction to Embedded Systems** [**08 Periods]**

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

MODULE - V: **Typical Embedded System** [**12 Periods]**

Core of the Embedded System: General Purpose and Domain Specific Processors, asics, plds, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

TEXT BOOKS:
1. Kenneth. J. Ayala, “The 8051 Microcontroller”, Cengage Learning, 3rd Edition, 2004. (Modules I, II & III)
2. Shibu K.V “Introduction to Embedded Systems”, Mc Graw Hill, 1st Edition, 2009. (Modules IV & V) 121

REFERENCE BOOKS:
1. Mazidi M.A, Mazidi JG, & Rolin D. Mckinlay, “The 8051 Microcontroller & Embedded Systems using Assembly and C”, Pearson Education, 2nd edition, 2007.
2. Frank Vahid, Tony Givargis, John Wiley, “Embedded System Design”, 2 nd edition, 2001.

OUTCOMES: After completion of the course, students will be able to:

1. Express architecture of Micro Controllers
2. Program a microcontroller system in assembly code and C.
3. Build and test a microcontroller-based system.
4. Understand the concepts of embedded systems.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4103	CMOS MIXED SIGNAL CIRCUIT DESIGN	L	T	P
Credits: 3		3	-	-

PREREQUISITES: CMOS Technology and Analog and Digital Communication Concepts.

OBJECTIVE: To Understand the design of circuits in IC form especially both digital and analog designs, to Understand the design of specific circuits like PLL,A/D,D/A and over sampling converters starts with Switched Capacitor circuits, to understanding the circuits by considering so many parameters may arises problems which need to be solve to get optimization

Module - I : SWITCHED CAPACITOR CIRCUITS [8 Periods]

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

Module – II : PHASED LOCK LOOP (PLL) [9 Periods]

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

Module - III : DATA CONVERTER FUNDAMENTALS [9 Periods]

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters-Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

Module - IV : NYQUIST RATE A/D CONVERTERS [8 Periods]

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time- interleaved converters.

Module - V : OVERSAMPLING CONVERTERS [7 Periods]

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibitquantizers, Delta sigma D/A

TEXT BOOKS:

1. Behzad Razavi, **Design of Analog CMOS Integrated Circuits,** TMH Edition, 2002

2.Philip E. Allen and Douglas R. Holberg, **CMOS Analog Circuit Design**, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. David A. Johns, Ken Martin, **Analog Integrated Circuit Design**, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. Rudy Van De Plassche, **CMOS Integrated Analog-to- Digital and Digital-to-Analog converters,** Kluwer Academic Publishers, 2003
2. Richard Schreier, **Understanding Delta-Sigma Data converters,** Wiley Interscience, 2005.
3. R. Jacob Baker, **CMOS Mixed-Signal Circuit Design,** Wiley Interscience, 2009.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. In a Position that he/she can design mixed signal-based circuits starting from basic constraints to advanced constraints
2. Design circuits like switched capacitor circuits, PLL, A/D and D/A converter
3. Understand the design of over sampling circuits and higher order modulators

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4110	VLSI DESIGN AND TECHNOLOGY	L	T	P
Credits: 3		3	-	-

PREREQUISITES: STLD and IC Technology

OBJECTIVE: To Understand the VLSI technology and design of circuits based on technology like cmos, bicmos etc, to understand the designing layouts of logic gates, to understanding the combinational logic networks and its optimization, to understanding the sequential systems and its optimization, to get knowledge on floor plan design

Module –I **[10 Periods]**

Crystal Growth and Wafer Preparation: Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Process Considerations.

Epitaxy: Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation.

Oxidation: Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopant At interface, Oxidation of Poly Silicon, Oxidation inducted Defects

Module –II **[9 Periods]**

Lithography: Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography.

Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes.

Module –III **[8 Periods]**

Dielectric and Polysilicon Film Deposition: Introduction, Deposition Processes, Polysilicon, Silicon Dioxide, Silicon Nitride, Plasma Assisted Depositions, Other Materials.

Diffusion: Models of Diffusion in Solids, Flick's one Dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques

Module -IV **[9 Periods]**

Ion Implantation: Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation.

Metallization: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization Problems..

Module -V **[8 Periods]**

MOS Technology: NMOS, PMOS, CMOS, BICMOS, Latch up,

Basic Electrical Properties of MOS and BICMOS circuits: Ids-V_{ds} relationships, MOS transistor threshold Voltage (Vt), Pass transistor, NMOS Inverter, Determination of pull-up to pull-down ratios, Various pull ups of MOS and BICMOS inverter, Lambda based Design Rules

Text Books:

1. S. M. Sze, "**VLSI Technology**", McGraw-Hill, Second Edition, 2003, TMH New Delhi.
2. Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, **Essentials of VLSI circuits and systems** –2005, PHI New Delhi.

Reference Books:

1. S.K. Ghandhi, "**VLSI Fabrication Principles**", John Wiley Inc., Second Edition New York, 1994.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Student will be in a position that he/she can design vlsi circuits starting from pmos nmos, cmos, and bicmos technology-based design
2. Gains thorough knowledge on design tools to draw layouts for the transistor structures
3. The student will understand the design of logic gates
4. The student will understand the design of sequential systems

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4111	ADVANCE DIGITAL SYSTEM DESIGN	L	T	P
Credits: 3		3	-	-

PREREQUISITES: VLSI and STLD

OBJECTIVE: To impart knowledge on the theory of Sequential machines and minimization of it. to design digital circuits for various applications. Thorough understanding of VHDL and modeling of digital systems using VHDL

MODULE – I :Minimization And Transformation Of Sequential Machines

[8 Periods]

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

MODULE – II : Digital Design [9 Periods]

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

MODULE – III: SM Charts [7 Periods]

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

MODULE – IV: Hardware Description Language [9 Periods]

Review of Verilog HDL, Modelling styles: Behavioural, Dataflow, and Structural Modelling, gate delays, switch-level Modelling, Hierarchal structural modelling, Design environment and constraints logic synthesizers, Language structure synthesis, coding guidelines for clocks and reset.

MODULE – V: Verification [8 Periods]

Functional verification, simulation types, Test Bench design, Dynamic timing analysis, static timing analysis. Design Examples-Adders and Subtractors, Multiplication and Division Algorithms, ALU.

TEXT BOOKS:

1. Charles H. Roth, **Fundamentals of Logic Design, Cengage** Learning,5th Ed.
2. Ming-Bo Lin., **Digital System Designs and Practices Using Verilog HDL and FPGAs,** Wiley, 2008.

3. J.Bhasker, **Verilog HDL Primer Hardcover,** 2nd Edition, Star Galaxy Publishing ,1999

REFERENCE BOOKS:

1. Michael D. Ciletti, **Advanced Digital Design with the Verilog HDL**", PHI, 2005.
2. Samir Palnitkar, "**Verilog HDL: A Guide to Digital Design and Synthesis**", Pearson Education, 2005.
3. John F Wakerley**, Digital Design Principles and Practice** ,4th Edition, Pearson education, 2006

COURSE OUTCOMES:

1. To expose the students to the fundamentals of sequential system design.
2. To enable the students to formulate and solve problems in Digital Systems design and implementation.
3. To develop Digital Systems design skills.
4. To make the students technically competent in design and implementation using VHDL

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4112	ALGORITHMS FOR VLSI DESIGN AUTOMATION	L	T	P
Credits: 3		3	-	-

PREREQUISITES: VLSI Design

OBJECTIVE: To study of basic and advanced algorithms used for VLSI CAD tools and To provide an introduction to the fundamentals of Computer-Aided Design tools for the modelling, design, analysis of digital Very Large Scale Integration (VLSI) systems

Module - I: [8 Periods]

Data structures for Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Spanning Tree Algorithm - Kruskal's and Prim's, Shortest path Algorithm - Dijkstra's and Bellman Fort Algorithm for single pair Shortest paths, Floyd-Warshall algorithm for All pair Shortest path, Matrix multiplication modelling of All pairs shortest path problem, Min cut and Max cut Algorithms

Module -II: [10 Periods]

Iintroduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis. Allocation , assignment and scheduling. Compaction: Problem formulation, one-dimensional compaction, two dimensions based compaction, hierarchical compaction.

Module - III: [10 Periods]

Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms
Placement, floor planning & pin assignment: Problem formulation, Placement algorithms, Floor planning concepts, Constraint based floor planning, Floor planning algorithms for mixed block & cell design, General & channel pin assignment.

Module - IV: [10 Periods]

Hardware Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.
Detailed routing: Problem formulation, single layer routing algorithms, two layers channel routing algorithms, three-layer channel routing algorithms, and switchbox routing algorithms

Module - V: [10 Periods]

PHYSICAL DESIGN AUTOMATION OF FPGAs: Band FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.
PHYSICAL DESIGN AUTOMATION OF MCMs: MCM technologies, MCM physical

design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing.

TEXT BOOKS:

1. Gerez, Sabih H. **Algorithms for VLSI design automation**, Vol. 8. New York: Wiley, 1999.
2. Sherwani, Naveed A. **Algorithms for VLSI physical design automation**, Springer Science & Business Media, 2012.

REFERENCE BOOKS:

1. Meinel, Meinel, Christoph, Thorsten Theobald, **Algorithms and data structures in VLSI design: OBDD-foundations and applications**, Springer Science & Business Media, 2012
2. Drechsler, Rolf, **Evolutionary algorithms for VLSI CAD**, Springer Science & Business Media, 2013.

COURSE OUTCOMES:

1 Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design

2 Demonstrate knowledge and understanding of fundamental concepts in CAD.

3 Demonstrate knowledge of computational and optimization algorithms and tool applicable to solving CAD related problems

4 Establish capability for CAD tool development and enhancement.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4113	EMBEDDED REAL-TIME OPERATING SYSTEMS	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Embedded System Concepts and Linux and UNIX Programming

OBJECTIVE: To learn fundamentals of UNIX operating system. To study implementation aspects of real time concepts. To study example RTOSs and applications.

Module - I: Introduction [8 Periods]

Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec.

Module - II: Real Time Operating Systems [9 Periods]

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

Module - III: Objects, Services and I/O [7 Periods]

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/OConcepts, I/O Subsystem

Module - IV: Exceptions, Interrupts and Timers [8 Periods]

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

Module - V: Case Studies of RTOS [9 Periods]

RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS and Basic Concepts of Android OS.

TEXT BOOKS:

1. Qing Li, **Real Time Concepts for Embedded Systems**, Elsevier, 2011

REFERENCE BOOKS:

1. Rajkamal, **Embedded Systems- Architecture, Programming and Design,**TMH, 2007,.
2. Richard Stevens, **Advanced UNIX Programming**,
3. Dr. Craig Hollabaugh , **Embedded Linux: Hardware, Software and Interfacing**

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Understand the fundamentals of UNIX operating system.
2. Understand the implementation aspects of real time concepts.
3. Understand the example RTOSs and applications.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4114	EMBEDDED PROGRAMMING	L	T	P
Credits: 3		3	-	-

PREREQUISITES: C Language, Linux and Embedded System Concepts

OBJECTIVE: Understand the significance of Linux and programming embedded C in real time applications and to use it for specific applications, to gain knowledge on 8051 micro controller, to develop code for real time embedded world, to understand design of real time timers with various constraints, to understand and gain knowledge on Intruder Alarm System.

UNIT – I: EMBEDDED OS FUNDAMENTALS (LINUX) [10 Periods]

Introduction: Operating System Fundamentals, General Linux Architecture, Linux Kernel, Linux file systems, ROOTFS, Sysfs and Procfs
Embedded Linux: Booting Process in Linux, boot loaders, U-boot, Kernel Images, Linux File systems.
Operating System Overview: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT – II: INTRODUCTION TO SOFTWARE DEVELOPMENT TOOLS[9 Periods]

GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools.

UNIT – III: EMBEDDED C PROGRAMMING [9 Periods]

Review of data types –scalar types-Primitive types-Enumerated types Subranges, Structure types-character strings –arrays- Functions
Introduction to Embedded C-Introduction, Data types Bit manipulation, Interfacing C with Assembly
Embedded programming issues - Reentrancy, Portability, Optimizing and testing embedded C programs.

UNIT – IV: EMBEDDED APPLICATIONS USING DATA STRUCTURES [12 Periods]

Linear data structures– Stacks and Queues Implementation of stacks and Queues- Linked List - Implementation of linked list, Sorting, Searching, Insertion and Deletion,
Nonlinear structures – Trees and Graphs
Object Oriented programming basics using C++ and its relevance in Embedded systems.

UNIT – V: SCRIPTING LANGUAGES FOR EMBEDDED SYSTEMS [9 Periods]

Shell scripting, Programming basics of Python, Comparison of scripting languages

TEXT BOOKS:

1. Michael J. Pont, **Embedded C**, Pearson Education, 2nd Ed,2008.

REFERENCE BOOKS:

1. Daniel W. Lewis, **Fundamentals of embedded software where C and assembly mee**t, Pearson Education, 2002.
2. Peter B. Galvin, Abraham Silberschatz, Gerg Gagne, **Operating System Concepts**, Wiley Publishers
3. Herbert Schildt, **The Complete Reference C++,** TMH
4. Bjarne Stoustrup, **C++ programming language**, Addison-Wesley
5. Tom Swan, **GNU C++ For Linux**, Prentice Hall India
6. Robert Lafore, **Object-oriented programming in C++,** Galgotia publications
7. Jones, M Tims, **GNU/LINUX Application Programming**,

COURSE OUTCOMES:

1. Develop advanced programs in Embedded C
2. Get knowledge in Embedded OS (Linux) fundamentals
3. Develop programs using scripting languages.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A4115	DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Digital Signal Processing

OBJECTIVE: To provide sound foundation of digital signal processing (DSP) architectures for designing efficient VLSI architectures for DSP systems. To analyse general purpose digital signal processors. To understand pipelining, parallel processing and retiming. To illustrate the features of on-chip peripheral devices and its interfacing along with its programming details. To analyse DSP architectures.

Module - I: INTRODUCTION TO DIGITAL SIGNAL PROCESSING[8 Periods]

Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT) Linear time-invariant systems, Digital filters, Decimation and interpolation

Module –II: COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS [9 Periods]

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Module- III: ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES [8 Periods]

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Module - IV: PROGRAMMABLE DIGITAL SIGNAL PROCESSORS [9 Periods]

Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, TMS320C54XX Instructions and Programming, On Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

Module - V: ANALOG DEVICES FAMILY OF DSP DEVICES [10 Periods]

Application Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor, Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, **Digital Signal Processing** –Thomson Publications, 2004.
2. K Padmanabhan, R. Vijayarajeswaran, S. Ananthi, **A Practical Approach to Digital Signal Processing** - New Age International, 2006/2009
3. Woon-Seng Gan, Sen M. Kuo, **Embedded Signal Processing with the Micro Signal Architecture**, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. B. Venkataramani and M. Bhaskar, **Digital Signal Processors, Architecture, Programming and Applications** –2002, TMH.

2. Jonatham Stein, **Digital Signal Processing**, John Wiley, 2005**.**

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. An ability to recognize the fundamentals of fixed- and floating-point architectures of various DSPs
2. An ability to learn the architecture details and instruction sets of fixed- and floating-point DSPs.
3. An ability to Infer about the control instructions, interrupts, and pipeline operations.
4. An ability to analyze and learn to implement the signal processing algorithms in DSPs.
5. An ability to learn the DSP programming tools and use them for applications.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. I Semester		
Code: A4104	MIXED SIGNAL DESIGN LAB	L	T	P
Credits: 2		-	-	4

NOTE: Following Experiments must be done using **Cadence / Mentor Graphics / Synopsys** Back End Tools and all types of Analysis must be carried out (Transient, AC Analysis, DC Analysis, Post Lay out & Pre Layout Simulations etc.)

List of experiments:

1. Current Source/Current Mirror Circuits
2. Common Source Amplifier
3. Class AB Amplifier
4. Feed Back Amplifier.
5. Differential Amplifier.
6. Trans conductance Operational Amplifier.
7. CMOS as a Comparator.
8. Analog Multiplier.
9. Switched Capacitor Integrator.
10. Sample and Hold Circuit.
11. Digital to Analog Converters (R-2R Ladder/Cyclic).
12. Phase Locked Loop.

Course Outcomes

CO1: Able to carry out research and development in the area of analog and mixed signal IC design.
CO2: To be well versed with the MOS fundamentals, small signal models and analysis of MOSFET based circuits.
CO3: Able to analyze and design analog circuits such as Differential Amplifier, OP-AMP, Current mirrors, Biasing circuits.
CO4: Able to analyze and design mixed mode circuits such as Comparator, PLL.
CO5: Solve practical and state of the art analog IC design problems to serve VLSI industries.

CO-PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

CO	Program Outcomes (POs)					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	3	1	
CO2	3	2	2	3	1	
CO3	3	2	2	3	1	
CO4	3	2	2	3	1	
CO5	3	2	2	3	1	

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. I Semester		
Code: A4105	EMBEDDED SYSTEM DESIGN LAB	L	T	P
Credits: 2		-	-	4

Note: The following programs are to be implement on 89C51 Development board using Embedded C Language on Keil IDE and Flash magic.

List of experiments:

1. Program to toggle all the bits of Port P1 continuously with 250 mS delay.
2. Program to toggle only the bit P1.5 continuously with some delay. Use Timer 0, mode 1 to create delay.
3. Program to interface a switch and a buzzer to two different pins of a Port such that the buzzer should sound as long as the switch is pressed.
4. Program to interface LCD data pins to port P1 and display a message on it.
5. Program to interface keypad. Whenever a key is pressed, it should be displayed on LCD.
6. Program to interface seven segment display unit.
7. Program to transmit a message from Microcontroller to PC serially using RS232.
8. Program to receive a message from PC serially using RS232.
9. Program to get analog input from Temperature sensor and display the temperature value on PC Monitor.
10. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise directions
11. Program to interfacing RFID.
12. Implementation of Traffic light controller.

Course Outcomes

CO1: Program a microcontroller system in assembly code and Embedded
CO2: Interface to peripherals, knowledge of typical interfacing standards
CO3: Development of prototype circuit on breadboard (including interfacing to microcontroller, and control from software)
CO4: Build and test a microcontroller-based system.
CO5: Understand the concepts of embedded systems

CO-PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

CO	Program Outcomes (POs)					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	3	1	
CO2	3	2	2	3	1	
CO3	3	2	2	3	1	
CO4	3	2	2	3	1	
CO5	3	2	2	3	1	

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech I Sem		
Code: A0A04	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P
Credits: Nil		2	-	-

Prerequisites: Nil

Course Objectives: The objective of the course is to provide the knowledge on structuring paragraphs, paraphrasing and preparation of research documents related to abstract, literature review, methods and results.

Module I **[6 Periods]**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Module II **[7 Periods]**

Clarifying Who Did What, Highlighting Your Findings, Hedging and criticising, paraphrasing and plagiarism, sections of a paper, abstracts. Introduction.

Module III **[6 Periods]**

Review of the Literature, Methods, Results, Discussion, Conclusions, the Final Check.

Module IV **[6 Periods]**

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Module V **[7 Periods]**

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

References:

1. Goldbort R, **Writing for Science**, Yale University Press, 2006
2. Day R, **How to Write and Publish a Scientific Paper**, Cambridge University Press, 2006
3. Highman N, **Handbook of Writing for the Mathematical Sciences**, SIAM. Highman's book, 1998.
4. Adrian Wallwork, **English for Writing Research Papers**, Springer New York Dordrecht Heidelberg London, 2011.

Course Outcomes:

At the end of the course, students will be able to

1. **Structure** the sentences and paragraphs.
2. **Elaborate** the various sections of research papers.

3. **Explore** the check list in research documents.
4. **Apply** the key skills to coin the title, abstract, introduction and literature review.
5. **Inspect** the skills required for preparing experimental results and discussions.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4106	CMOS DIGITAL IC DESIGN	L	T	P
Credits: 3		3	-	-

PREREQUISITES: VLSI Technology and IC Design

OBJECTIVE: To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits, Sequential MOS logic circuits, To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Module - I **[10 Periods]**

MOS DESIGN: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

Module - II **[8 Periods]**

COMBINATIONAL MOS LOGIC CIRCUITS:MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Module - III **[7 Periods]**

SEQUENTIAL MOS LOGIC CIRCUITS: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

Module - IV **[10 Periods]**

DYNAMIC LOGIC CIRCUITS: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Module - V **[8 Periods]**

SEMICONDUCTOR MEMORIES: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS

1. Ken Martin**, Digital Integrated Circuit Design**, Oxford University Press, 2011.
2. Sung-Mo Kang, Yusuf Leblebici, **CMOS Digital Integrated Circuits Analysis and Design,** TMH, 3rd Ed., 2011.

REFERENCE BOOKS

1. Ming-BO Lin, **Introduction to VLSI Systems: A Logic, Circuit and System Perspective**, CRC Press, 2011

2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, **Digital Integrated Circuits – A Design Perspective,** 2nd Ed,PHI.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Able to understand the realization of different logic circuit designs for logic expressions and the importance of the circuit designs, the drawback of the designs both in combinational as well as sequential.
2. Able to know different types of memories, performance evaluation of each memory modules they can be able to think how to improve performance by taking different structures

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4107	ADVANCE EMBEDDED PROCESSORS	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Microcontrollers and Embedded Systems

OBJECTIVE: To know about ARM Processors Registers, Instruction pipeline, Interrupts and Architecture, to learn about Instructions, Addressing modes and conditional instructions, to learn about Cache architecture, Polices, Flushing, MMU, page tables, translational, and access permissions.

Module- I: ARM ARCHITECTURE [10 Periods]

ARM Register set ,Modes , Interrupt vector Table , ARM Assembly programming using the Keil RVDK tool ,ARM Instruction set ,Conditional Execution ,Arithmetic instructions, Logical Instructions, Branch instructions, Load and Store instructions, Multiple load//store instructions, Realization of stacks..

Module - II: PERIPHERAL PROGRAMMING [9 Periods]

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

Module - III: ARM9 MICROCONTROLLER ARCHITECTURE [10 Periods]

AT91RM9200 Architecture: Block Diagram, Features, Memory Mapping
Memory Controller (MC): Memory Controller Block Diagram, Address Decoder, External Memory Areas, Internal Memory Mapping
External Bus Interface (EBI): Organization of the External Bus Interface, EBI Connections to Memory Devices
External Memory Interface: Write Access, Read Access, Wait State Management

Module - IV: AT91RM9200 PERIPHERALS [9 Periods]

Interrupt Controller: Normal Interrupt, Fast Interrupt, AIC
System Timer (ST): Period Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT), Real Time Clock (RTC) Parallel Input/output Controller (PIO)

Module - V: CORTEX-M3/M4 MICROCONTROLLER [7 Periods]

STM32L15xxx ARM Cortex M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control.
STM32L15xxx Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART.

TEXT BOOKS:

1. Andrew N.Sloss, Dominic Symes, Chris Wright, **ARM Systems Developer's Guides- Designing & Optimizing System Software**, Elsevier, 2008.
2. Lyla B.Das: "Embedded Systems -An Integrated Approach", Pearson Education , India, 2012.
3. Joseph Yiu, **The Definitive Guide to the ARM Cortex-M3**, Second Edition, Elsevier Inc. 2010.

REFERENCE BOOKS:

1. Jonathan W. Valvano – Brookes/ Cole, **Embedded Microcomputer Systems, Real Time Interfacing**, Thomas Learning, 1999.
2. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual
3. David Seal, **ARM Architecture Reference Manual**, 2001 Addison Wesley England; Morgan Kaufmann Publishers.
4. Andrew N Sloss, Dominic Symes, Chris Wright, **ARM System Developer's Guide - Designing and Optimizing System Software**, 2006, Elsevier

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. To understand architecture and features of typical Microcontroller.
2. To understand architecture, features and need of ARM7& ARM CORTEX processors in embedded system.
3. To learn peripheral programming with ARM7& ARM CORTEX processors.
4. To understand architecture, features and external interfaces of ARM 9 Microcontrollers

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4116	DESIGN OF FAULT TOLERANT SYSTEMS	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Digital System Design with PLDS**.**

OBJECTIVE: To provide or broad understanding of fault diagnosis and tolerant design Approach. To illustrate the framework of test pattern generation using semi and full automatic approach.

MODULE-I: Fault Tolerant Design [12 Periods]

Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits. Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

MODULE -II: Self Checking circuits & Fail safe Design [12 Periods]

Self checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code. Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design.

MODULE-III: Design for Testability [12 Periods]

Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.

Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architecturesfull scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

MODULE-IV: Logic Built-in-self-test [12 Periods]

Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test (BEST), Random Test socket(RTS), LSSD On-chip self test, Self – testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

MODULE-V: Standard IEEE Test Access Methods [12 Periods]

Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.

TEXT BOOKS:

1. Parag K. Lala, **"Fault Tolerant & Fault Testable Hardware Design",** 1984, PHI.
2. Zainalabedin Navabi, **"Digital System Test and Testable Design using HDL models and Architectures",** Springer International Edition

REFERENCE BOOKS:

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, **"Digital Systems Testing and Testable Design**", Jaico Books.
2. Bushnell & Vishwani D. Agarwal, "**Essentials of Electronic Testing",** Springer
3. Alfred L. Crouch, "**Design for Test for Digital IC's and Embedded Core Systems",** 2008, Pearson Education.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. To acquire the knowledge of fundamental concepts in fault tolerant design.
2. Design requirements of self check-in circuits
3. Test pattern generation using LFSR
4. Design for testability rules and techniques for combinational circuits
5. Introducing scan architectures.
6. Design of built-in-self test.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4117	LOWER POWER VLSI DESIGN	L	T	P
Credits: 3		3	-	-

PREREQUISITES: VLSI Technology and Design

OBJECTIVE: To Identify suitable techniques to reduce the power dissipation. To learn design of adders, multipliers and memory circuits with low power dissipation

Module - I **[10 Periods]**

FUNDAMENTALS: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects – Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

Module - II **[10 Periods]**

LOW-POWER DESIGN APPROACHES:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

Module - III **[9 Periods]**

LOW-VOLTAGE LOW-POWER ADDERS: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

Module - IV **[8 Periods]**

LOW-VOLTAGE LOW-POWER MULTIPLIERS: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

Module – V **[8 Periods]**

LOW-VOLTAGE LOW-POWER MEMORIES: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Sung-Mo Kang, Yusuf Leblebici, **CMOS Digital Integrated Circuits – Analysis and Design**, TMH, 2011.
2. Kiat-Seng Yeo, Kaushik Roy, **Low-Voltage, Low-Power VLSI Subsystems**

–TMH Professional Engineering.

REFERENCE BOOKS:

1. Ming-BO Lin, **Introduction to VLSI Systems: A Logic, Circuit and System Perspective**, CRC Press, 2011
2. **Low Power CMOS Design**, Anantha Chandrakasan, IEEE Press/Wiley International, 1998.
3. Kaushik Roy, Sharat C. Prasad, **Low Power CMOS VLSI Circuit Design – John Wiley & Sons**, 2000.
4. Gary K. Yeap, **Practical Low Power Digital VLSI Design**, Kluwer Academic Press, 2002.
5. A. Bellamour, M. I. Elamasri, **Low Power CMOS VLSI Circuit Design**, Kluwer Academic Press, 1995.
6. Siva G. Narendran, Anatha Chandrakasan, **Leakage in Nanometer CMOS Technologies, Springer**, 2005.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Clearly identify the sources of power consumption, analyze and estimate leakage power components in a given VLSI circuit.
2. Choose different types of SRAMs/DRAMs for low power applications.
3. Design low power arithmetic circuits and systems.
4. Decide at which level of abstraction it is advantageous to implement low power techniques in a VLSI system design.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4118	CPLD AND FPGA ARCHITECTURES AND APPLICATIONS	L	T	P
Credits: 3		3	-	-

PREREQUISITES: STLD and VLSI

OBJECTIVE: To understand the types of programmable logic devices and what are the differences between these devices. What are the different complex programmable logic devices with examples, to know the types of FPGA's and their programming technologies. What are the programmable logic block architectures, their interconnects and what are applications of FPGA's, to understand about the SRAM programmable FPGA's and their programming technology. What are examples of SRAM programmable FPGA's i.e Xilinx FPGA's with block diagrams.

Module - I: Introduction to Programmable Logic Devices [10 Periods]
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

Module –II: Field Programmable Gate Arrays [9 Periods]
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

Module – III : SRAM Programmable FPGSs [8 Periods]
Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 andXC4000 Architectures.

Module -IV: Anti-Fuse Programmed FPGAs [8 Periods]
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

Module – V: Design Applications [9 Periods]
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, Field **Programmable Gate Array Technology**,Springer International Edition.
2. Charles H. Roth Jr, Lizy Kurian John, **Digital Systems Design**, Cengage Learning.

REFERENCE BOOKS:

1. John V. Oldfield, Richard C. Dorf, **Field Programmable Gate Arrays**, Wiley India.
2. Pak K. Chan/Samiha Mourad, **Digital Design Using Field Programmable**

Gate Arrays, Pearson Low Price Edition.
3. Ian Grout, Elsevier, **Digital Systems Design with FPGAs and CPLDs**, Newnes.
4. Wayne Wolf, **FPGA based System Design**, Prentice Hall Modern Semiconductor Design Series.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. The students will have the knowledge of types of programmable logic devices and what are the differences between these devices.
2. The students will have the knowledge of types of FPGA's and their programming technologies, programmable logic block architectures, their interconnects and what are applications of FPGA's.
3. The students will be able to know the programming technology of SRAM programmable FPGA's with their internal logic diagram.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4119	HARDWARE AND SOFTWARE CO-DESIGN	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Concepts of Models and Architectures

OBJECTIVE: To design mixed hardware-software systems and the design of hardware-software interfaces, To focus on common underlying modeling concepts, and the trade-offs between hardware and software components, To learn about System –level specification, design representation for system level synthesis, system level specification languages.

Module –I: Co-Design Issues [10 Periods]

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- synthesis algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co synthesis.

Module –II: Prototyping and Emulation [8 Periods]

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

Module –III: Compilation Techniques and Tools for Embedded Processor Architectures [8Periods]

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

Module –IV: Design Specification and Verification [10 Periods]

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

Module –V: Languages for System – Level Specification and Design-I [9 Periods]

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for system – level specification and design-ii: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycossystem.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, **Hardware / Software Co- Design Principles and Practice**, Springer, 2009.

2. Giovanni De Micheli, Mariagiovanna Sami, **Hardware / Software Co- Design**

,KluwerAcademic Publishers,2002.

REFERENCE BOOKS:

1. Patrick R. Schaumont, **A Practical Introduction to Hardware/Software Co-design**, Springer,2010.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Able to design mixed hardware-software systems and the design of hardware-software interfaces
2. Able to focus on common underlying modeling concepts and the trade-offs between hardware and software components.
3. Able to learn about System –level specification, design representation for system level synthesis, system level specification languages.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4120	EMBEDDED NETWORK CONTROLLERS	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Microcontrollers and Computer Networks

OBJECTIVE: To understand the significance of embedded networks in real time applications and to use it for specific applications, to Know different types of communication protocols like serial and parallel communication protocols, to know different types of communication protocols which have embedded end modules, to understand wired and wireless communication protocols, its formats ,to understand and gain knowledge on wireless sensors and its application in wireless embedded networks

Module - I: Embedded Communication Protocols [8 Periods]

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols –Firewire.

Module - II: USB and CAN Bus [10 Periods]

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames – Bit stuffing –Types of errors –Nominal Bit Timing –PIC microcontroller CAN Interface –A simple application with CAN.

Module - III: Ethernet Basics [9 Periods]

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers –Using the internet in local and internet communications – Inside the Internet protocol.

Module - IV: Embedded Ethernet [8 Periods]

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

Module - V: Wireless Embedded Networking [8 Periods]

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing –Data Centric routing.

TEXT BOOKS:

1. Frank Vahid, Tony Givargis, **Embedded Systems Design: A Unified Hardware/Software Introduction,** John & Wiley Publications, 2002
2. Jan Axelson, **Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port,** Penram Publications, 1996.

REFERENCE BOOKS:

1. Dogan Ibrahim, **Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series**, Elsevier 2008.
2. Jan Axelson, **Embedded Ethernet and Internet Complete,** Penram publications, 2003.
3. Bhaskar Krishnamachari, **Networking Wireless Sensors,** Cambridge press 2005.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Understand the basic working modes of networks and its formatted data frames, its control
2. Understand the significance of embedded networks in real time applications and to use it for specific applications.
3. Know different types of communication protocols like serial and parallel communication protocols
4. Know different types of communication protocols which have embedded end modules
5. Understand wired and wireless communication protocols, its formats
6. Understand and gain knowledge on wireless sensors and its application in wireless embedded networks

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A4121	SYSTEM ON-CHIP ARCHITECTURE	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Computer Architecture, Digital circuits and Embedded Systems.

OBJECTIVE: This course introduce to computer system design, with emphasis on fundamental ideas and analytical techniques that are applicable to a range of applications and architectures. This course introduces hardware and software programmability verses performance. This course introduces of entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices.

Module – I: Introduction to The System Approach
[08Periods]
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, an approach for SOC Design, System Architecture and Complexity.

Module – II: Processors [12 Periods]
Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Module – III: Memory Design for Soc
[10Periods]
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

Module – IV: Interconnects Customization and Configuration
[12Periods]
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Module – V: APPLICATION STUDIES / CASE STUDIES [08 Periods]
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, **"Computer System Design System on Chip"**, Wiely India Pvt. Ltd., 2012. (Modules I, II, III, IV & V)

REFERENCE BOOKS:

1. Steve Furber**, "ARM System on Chip Architecture",** Addison Wesley Professional, 2nd Edition, 2000.
2. Ricardo Reis, **"Design of System on a Chip: Devices and Components"**, Springer, 1st Edition, 2004.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Know how the system forms with the lot of component and has majority about system level interconnections
2. Understand hardware and software programmability verses performance
3. Know about entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. II Semester		
Code: A0H11	RESEARCH METHODOLOGY AND IPR	L	T	P
Credits: 2		2	-	-

PREREQUISITES: Nil

Course Objectives: The objective of the course is to make students familiar with the basics of research methodology and various types of Intellectual Properties, IPR legislations and policies.

Module I: Research Problem **[6 Periods]**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

Module II: Technical Writing and Research Proposal **[7 Periods]**

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Module III: Intellectual Property Rights **[6 Periods]**

A: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. **B:** International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Module IV: Patent Rights **[6 Periods]**

Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Module V: Case Studies **[7 Periods]**

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

1. Prabhuddha Ganguli, **Intellectual Property Rights**, Tata Mc-Graw – Hill, New Delhi
2. M. Ashok Kumar and Mohd. Iqbal Ali, **Intellectual Property Right,** Serials Pub.
3. Carlos M.Correa, **Intellectual property rights**, The WTO and Developing countries"-Zed books
4. Wadehra, B.L, **Law relating to patents, trademarks**, copyright designs. & 2 ed. Universal Law Publishing 2000.
5. C.R.Kothari, **Research Methodology**, New Age International

Publishers, Fourth edition, 2018.
6. Donald Cooper & Pamela Schindler, **Business Research Methods**, TMGH, 9th edition.
7. Alan Bryman & Emma Bell, **Business Research Methods**, Oxford University Press.

Course Outcomes:

After completion of the course, students will be able to:

1. Comprehend the concepts of research methodology and its concepts.
2. Realize the concepts of literature review and developing a research proposal.
3. Understand the basic concepts of Intellectual property rights.
4. Understand the types of patents and their procedures.
5. Recognize the recent developments in IPR administration.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)			M.Tech. II Semester
Code: A4108	DIGITAL IC DESIGN LAB	L	T	P
Credits: 2		-	-	4

Note: Programming can be done using any complier. Down load the programs on XILINX FPGA/CPLD boards.

List of Experiments:

1. HDL code to realize all the logic gates
2. Design and Simulation of half adder, full adder, parallel adder and Serial Binary Adder.
3. Design of decoders and encoders.
4. Design of Multiplexer/ De multiplexer, comparator
5. Design of flip flops: SR, D, JK, T
6. Design of 4-bit binary, BCD counters.
7. Design of a N- bit universal shift register.
8. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
9. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication, and Division.

Note: Layout, Physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following using Cadence / Mentor Graphics / Synopsys tools:

10. CMOS Inverter.
11. CMOS NOR/ NAND Gates.
12. CMOS 1-bit Full Adder.

Course Outcomes

CO1: Design synchronous and Asynchronous sequential circuits using Verilog HDL/ VHDL
CO2: Develop soft methods for identifying faulty digital circuits
CO3: Synthesize digital circuit using Verilog HDL/ VHDL
CO4: Design combinational and sequential circuits at circuit level
CO5: Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits.

CO-PO Mapping
(3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak

CO	Program Outcomes (POs)					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	3	1	
CO2	3	2	2	3	1	
CO3	3	2	2	3	1	
CO4	3	2	2	3	1	
CO5	3	2	2	3	1	

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. II Semester		
Code: A4109	ADVANCED EMBEDDED SYSTEM LAB	L	T	P
Credits: 2		-	-	4

Note: The following programs are to be implement on ARM based Processors using Keil IDE and Flash magic.

List of experiments:

1. Introduction to ARM Development Board & Software
2. Simple Assembly Program for
   a. Addition | Subtraction | Multiplication |Division
3. Simple Assembly Program for
   a. Operating Modes, System Calls and Interrupts
   b. Loops, Branches
4. Write an Assembly programs to configure and control General Purpose Input/output (GPIO) port pins.
5. Write an Assembly programs to read digital values from external peripherals and execute them with the Target board.
6. Program to demonstrate Time delay program using built in Timer / Counter feature on IDE environment
7. Program to demonstrates a simple interrupt handler and settingup a timer
8. Program demonstrates setting up interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal.
9. Program to Interface 8 Bit LED and Switch Interface
10. Program to implement Buzzer Interface on IDE environment
11. Program to Displaying a message in a 2-line x 16 Characters LCD display and verify the result in debug terminal.
12. Demonstration of Serial communication. Transmission from Kit and reception from PC using Serial Port on IDE environment use debug terminal to trace the program

Course Outcomes

CO1: Program a Advanced microcontroller system in assembly code and Embedded C
CO2: To learn peripheral programming with ARM7& ARM CORTEX processors
CO3: Development of prototype circuit on breadboard (including interfacing to microcontroller, and control from software)
CO4: Build and test a microcontroller-based system.
CO5: To design mixed hardware-software systems and the design of hardware software interfaces

CO-PO Mapping (3/2/1 indicates strength of correlation) 3-Strong, 2-Medium, 1-Weak						
CO	Program Outcomes (POs)					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2	2	3	1	
CO2	3	2	2	3	1	
CO3	3	2	2	3	1	
CO4	3	2	2	3	1	
CO5	3	2	2	3	1	

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech II Sem		
Code: A0A05	VALUE EDUCATION	L	T	P
Credits: Nil		2	-	-

Prerequisites: Nil

Course Objectives: The course deals about value of education and self-development, Imbibe good values in students and know about the importance of character.

Module I **[6 Periods]**

Values and self-development -Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements.

Module II **[7 Periods]**

Importance of cultivation of values, Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness, Honesty, Humanity. Power of faith, National Unity, Patriotism. Love for nature, Discipline.

Module III **[6 Periods]**

A:Personality and Behavior Development - Soul and Scientific attitude, Positive Thinking. Integrity and discipline, Punctuality,

B: Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour.

Module IV **[7 Periods]**

Universal brotherhood and religious tolerance, True friendship Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature.

Module V **[6 Periods]**

Character and Competence -Holy books vs Blind faith, Self-management and Good health Science of reincarnation, Equality, Nonviolence ,Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively.

References:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

Course Outcomes:

After completion of the course, students should be able to:

1. **Understand** self-development and moral values

2. **Explore** the importance of character and cultivation of values
3. **Apply** the personality development methods
4. **Analyze** the association and cooperation principles
5. **Elaborate** the principles of religions and good health science.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)			M.Tech III Sem
Code: A4122	IMAGE AND VIDEO PROCESSING	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Signal Processing.

OBJECTIVE: To Study fundamental concepts of Image Processing and various Image Transforms. Learn Image Enhancement Techniques in Spatial domain, Image Segmentation methods. To Familiarize with fundamentals of Image compression, Lossy & Lossless Compression methods. Define concepts of Video Processing, Image Formation models, and processing of Video signals. Understand general methodologies of 2 D Motion Estimation and Video coding methods.

UNIT -I: FUNDAMENTALS OF IMAGE PROCESSING [8 Periods]

Basic steps of Image Processing System, Sampling and Quantization of an image, relationship between pixels.

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, smoothing spatial filters, Sharpening spatial filters

UNIT -II: IMAGE SEGMENTATION [10 Periods]

Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation, Hough Transform, Boundary detection, chain coding.

Image Restoration: A Model of the Image Degradation/Restoration Process, inverse filtering, wiener filtering, Constrained Least Squares Filtering, geometric transformation.

Color Image Processing: color models, pseudo coloring, Color Segmentation, Color Image Compression.

UNIT -III: IMAGE COMPRESSION [9 Periods]

Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT -IV: BASIC CONCEPTS OF VIDEO PROCESSING [8 Periods]

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT -V: 2-D MOTION ESTIMATION [10 Periods]

Optical flow, General Methodologies, Pixel Based Motion Estimation, BlockMatching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding,

Application of motion estimation in Video coding, constant dependent video coding and joint shape and texture coding .MPEG and H.26X standards.

TEXT BOOKS:

1. Gonzaleze and Woods, **Digital Image Processing**, 3rd edition, Pearson.
2. Yao Wang, Joem Ostermann, Ya–quin Zhang, **Video processing and communication**, 1st Edition, PH Int
3. S.Jayaraman, S.Esakkirajan, T.Veera Kumar, **Digital Image Processing**, TMH, 2009.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Understand, analyze and develop new image processing problems and algorithms.
2. Help in designing the hardware architecture for image processing algorithms
3. Develop the skill to further explore the advanced topics of digital image processing

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech III Sem		
Code: A4123	SENSORS AND ACTUATORS	L	T	P
Credits: 3		3	-	-

PREREQUISITES: Embedded Systems Sensors and Sensor, Actuators Types.

OBJECTIVE: To learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization, to know about different sensors like Thermal sensors, Magnetic sensors, to know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

Module -I: Sensors/ Transducers [8 Periods]

Principles–Classification–Parameters–Characteristics–EnvironmentalParameters (EP) – Characterization.

Mechanical and electromechanical sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors: – Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors

Module -II: Thermal Sensors [10 Periods]

Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors– Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermo sensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermo emf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors

Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors –Anisotropic Magneto resistive Sensing – Semiconductor Magneto resistors– Hall Effect and Sensors –Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros –Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flow meter – Switching Magnetic Sensors SQUID Sensors

Module -III: Radiation and Electro Analytical Sensors [9 Periods]

Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.

Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

Module -IV: Smart Sensors and Applications [9 Periods]

Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation.

Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring

Module -V: Actuators [10 Periods]

Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems - Mechanical switches – Solid-state switches
Solenoids – D.C. Motors – A.C. motors – Stepper motors

TEXT BOOKS:

1. D. Patranabis, **Sensors and Transducers,** PHI Learning Private Limited.
2. W. Bolton, **Mechatronics,** Pearson Education Limited.

REFERENCE BOOKS:

1. D. Patranabis**, Sensors and Actuators,** PHI, 2nd Ed, 2013.

COURSE OUTCOMES:

After completion of the course, students will be able to:

1. Learn about sensor Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), and Characterization.
2. Know about different sensors like Thermal sensors, Magnetic sensors.
3. Know about Smart Sensors, Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface and the Automation

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech III Sem		
Code: A4124	WIRELESS SENSOR NETWORKS	L	T	P
Credits: 3		3	-	-

Pre-requisites: Embedded network controllers.

OBJECTIVE: To impart knowledge about wireless sensor networks and its application area. To introduce the fundamental concepts relevant to deployment and localization of wireless sensor networks. To enable the students to understand the synchronization and dissemination of information using wireless sensor network about the target area

Module – I: Introduction [9 Periods]
The Vision, Networked Wireless Sensor Devices, Applications of Wireless Sensor Networks, Key Design Challenges,
Network Deployment: Structured Versus Randomized Deployment, Network Topology, Connectivity in Geometric Random Graphs, Connectivity using Power Control, Coverage Metrics, Mobile Deployment,

Module – II: Localization and Time Synchronization [12 Periods]
Localization: Key Issues, Localization Approaches, Coarse-Grained Node Localization Using Minimal Information, Fine-Grained Node Localization Using Detailed Information, Network- Wide Localization, Theoretical Analysis of Localization Techniques,
Time Synchronization: Key Issues of Time Synchronization, Traditional Approaches, Fine-Grained Clock Synchronization, Coarse grained Data Synchronization.

Module – III: Wireless Characteristics and Medium-Access [9 Periods]
Wireless Link Quality, Radio Energy Considerations, The SINR Capture Model for Interference, Traditional MAC Protocols, Energy Efficiency in MAC Protocols, Asynchronous Sleep Techniques, Sleep-Scheduled Techniques, and Contention-Free Protocols.

Module – IV: Sleep-Based Topology Control & Energy-Efficient Routing [9 Periods]
Constructing Topologies for Connectivity, Constructing Topologies for Coverage, Set K-cover Algorithms, Cross-Layer Issues, Metric-Based Approaches, Routing with Diversity, Multi-Path Routing, Lifetime-Maximizing Energy-Aware Routing Techniques, Geographic Routing, Routing to Mobile Sinks.

Module – V: Data-Centric Networking [9 Periods]
Data-Centric Routing, Data-Gathering with Compression, Querying, Data-Centric Storage and Retrieval, Database Perspective on Sensor Networks,
Transport Reliability and Congestion Control: Basic Mechanisms and Tunable Parameters, Reliability Guarantees, Congestion Control, Real-Time Scheduling.

Text Books :

1. Bhaskar Krishnamachari, **Networking Wireless Sensors**, Cambridge University Press.
2. Feng Zhao and Leonidas Guibas, **Wireless Sensor Networks-An Information Processing**

Approach, Morgan Kauffman.
3. K. Sohraby, D. Minoli and T. Znati, **Wireless Sensor Networks Technology, Protocols and Applications**, John Wiley & Sons.

COURSE OUTCOMES:

At the end of the course the student will be able to:

1. Understand Have an understanding of the principles and characteristics of wireless sensor networks.
2. Apply knowledge of wireless sensor networks to various application areas.
3. Analyze WSN protocols in terms of their energy efficiency and design new energy efficient protocols

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech III Sem		
Code: A5128	BUSINESS ANALYTICS (Open Elective)	L	T	P
Credits: 3		3	-	-

Prerequisites: Nil

Course Objectives:

This course provides the students to learn and understand the role of business analytics within an organization, Analyze data using statistical and data mining techniques Also to gain an understanding of how managers use business analytics to formulate and solve, business problems.

Module I: **Business analytics and Statistical Tools** **[9 Periods]**

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business, Analytics Process and organization, competitive advantages of Business Analytics.

Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modeling, sampling and estimation methods overview.

Module II: **Trendiness and Regression Analysis** **[9 Periods]**

Modeling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

Module III: **Organization Structures and Analytics** **[10 Periods]**

A: Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, measuring contribution of Business analytics, Managing Changes.

B: Descriptive Analytics, predictive analytics, predicative Modeling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modeling, nonlinear Optimization.

Module IV: **Forecasting Techniques** **[10 Periods]**

Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

Module V: **Decision Analysis** **[10 Periods]**

Formulating Decision Problems, Decision Strategies with the without outcome Probabilities, Decision Trees, Value of Information, Utility and Decision Making. Recent

Trends in Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

TEXT BOOKS

1. Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, "**Business analytics Principles, Concepts, and Applications**"**,** Pearson FT Press.
2. James Evans, "**Business Analytics**"**,** Persons Education.

REFERENCES

1. James Cadle, Donald Yeates, James Cadle, Malcolm Eva, Keith Hindle, Debra Paul, Craig Rollason, Paul Turner, Donald Yeates Debra Paul, "**Business Analysis**"**,** BCS, The Chartered Institute for IT; Revised edition, 2014.
2. Erik Larson and, Clifford Gray**, "Project Management: The Managerial Process**", McGraw Hill Education; Sixth Edition, 2017.

Course Outcomes:

At the end of the course, students will be able to:

1. **Understand** the knowledge and need for data analytics.
2. **Demonstrate** the ability of think critically in making decisions based on data and deep analytics.
3. **Explore** the technical skills in predicative and prescriptive modeling to support business decision-making.
4. **Acquire** the ability to translate data into clear, actionable insights.
5. **Analyze** the problems and use various decision strategies.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. III Semester		
Code: A0B20	ADVANCED OPTIMIZATION TECHNIQUES (Open Elective)	L	T	P
Credits: 3		3	-	-

Pre-requisite: Nil

Course Objectives:

To understand extremely important topics under the broad umbrella of optimization, this is synonymous with efficiency which is the underlying prime rationale for all scientific and technological advances and progress.

Module I: Linear Programming [10 Periods]

Introduction and formulation of models; convexity; graphical &simplex method; Big-M Method, Two phase method; degeneracy, non-existent and unbounded solutions; duality in L.P. Dual simplex method, sensitivity analysis for cost and requirement vector; Revised simplex method; Transportation and Assignment problems.

Module II: Integer Linear Programming [10 Periods]

Gomory's cutting plane method; branch and bound algorithm; traveling salesman problem; knapsack problem; linear C-1 problem.

Module III: Dynamic Programming, CPM & PERT [9 Periods]

A: Belman's Principle of optimality; recursive relations; Solution of L.P. Problem; simple examples.

B: CPM & PERT

Module IV: Non-Linear Programming [9 Periods]

Classical optimization methods; equality and inequality constraints; Lagrange multipliers; Kuhn-tucker conditions; quadratic forms; quadratic programming and Beale's methods.

Module V: Search Methods [10 Period]

One dimensional optimization; Fibonacci search; multi dimensional search methods; uni-variate search; gradient methods; steepest descent/ascent methods; conjugate gradient method; Fletcher- reeves method; penalty function approach.

TEXT BOOKS

1. J.K. Sharma, "**Operations Resarach Theory & Applications**", 4th Edition, Mc.Millan Publications
2. S.S.Rao, "**Engineering Optimization theory and Practice**", 4th Edition, J Wiley & Sons, Newjersey

REFERENCES

1. K.V.Mital , **"Optimization methods in operations research and system analysis**", 3rd Edition, Newage International (P) Ltd., publishers.
2. H.A Taha "**Operations Research: An Introduction**" Prentice Hall Edition, 2016

reprint
3. Raul Poler et.al “Operations Research Problems Statement and solutions” Springer, 2014.

Course Outcomes

After completion of the course, students will be able to:

1. Find feasible solution to LPP by various methods.
2. Minimize the cost and time by using Travelling salesmen Problem.
3. Understand various methods Dynamic programming.
4. Understand the various concepts on Non-Linear programming.
5. Understand the various concepts of Search methods.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. III Semester		
Code: A3228	**INDUSTRIAL SAFETY** (Open Elective)	**L**	**T**	**P**
Credits: 3		**3**	**-**	**-**

Prerequisites: Industrial Management

Course objectives: The objective of this course is to understand and maintain health and safety from various hazards and understand the different types of maintenance in industry.

Module-I: Industrial safety **10 Periods**

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

Module -II: Fundamentals of maintenance engineering: **9 Periods**

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Module -III: Wear and Corrosion and their prevention: **9 Periods**

A: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, Screw down grease cup, Pressure grease gun,. Splash lubrication, Gravity lubrication, Wick feed lubrication, Side feed lubrication and Ring lubrication.

B: Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Module-IV: Fault tracing: **10 Periods**

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Module -V: Periodic and preventive maintenance: 10 Periods

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Text Books:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

References:

1. Pump-hydraulic Compressors, Audels, McGraw Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

E-Resources

1. https://www.safeopedia.com/definition/1052/industrial-safety
2. https://en.wikipedia.org/wiki/Industrial_safety_system

Course Outcomes

After completion of the course, students will be able to:

1. Understand the basic concepts of industrial safety needs
2. Understand and identify various hazards in industry
3. Understand and avoid wear and tear during manufacturing process
4. Identify suitable fault-finding activities
5. Use periodic and preventive maintenance in industry

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. III Semester		
Code: A0522	INTERNET OF THINGS (Open Elective)	L	T	P
Credits: 3		3	-	-

Prerequisites: Basic knowledge of computer architecture, programming and communication protocols

Course objectives: Understand the basics of Embedded System, IoT and the development model. Understand the architecture, Instruction set and work on ARM microcontroller using practical hands-on. Ability to select appropriate hardware and microcontrollers based on need of application. Understand the Internet of Things Standards, Frameworks and Techniques. Apply the tools, techniques and skills acquired towards development of Projects.

Module-I: Introduction to Embedded Systems and Internet of Things (IOT) 9 Periods

Architecture of Embedded Systems , Embedded Systems Development process, Architecture of Internet of Things , Applications of Embedded Systems and IoT, Design Methodology for IOT Products.

Module -II: Overview of Open Source Hardware and Its relevance to IOT 9 Periods

Introduction and Programming Arduino Development Board , Working with Sensor Integration, Interfacing Input / Output devices (Pot, LDR, LCD, etc), Introduction to Network Connectivity, Concepts of IP based communication, Client – Server model of communication, Introduction to Wi-Fi communication using ESP8266, ESP8266 in Station & Access Point Mode.

Module -III: Fundamentals of Python Programming & Raspberry PI 10 Periods

A: Introduction to python programming, working with functions, classes, REST full Web Services, Client Libraries.
B: Introduction & programming Raspberry Pi3, Integrating Input Output devices with Raspberry Pi3.

Module-IV: IOT Platform: Cloud Computing Platforms for IOT Development (IBM Cloud) 10 Periods

IOT Platform Architecture (IBM Internet of Things & Watson Platforms), API Endpoints for Platform Services , Devices Creation and Data Transmission, Introduction to NODE-RED and Application deployment.

Module -V: IOT Usecases: Smart city Project & Industrial Usecases **10 Periods**

Introduction to Smart City Project & IOT Use cases , Development of Smart city Applications , Project Work -1 (Smart city Use case) , Project Work-2 (Industrial Use case)

Text Books:

1. Internet of Things: A Hands-On Approach by by Arsheep Bahga, Vijay Madisetti
2. The Internet of Things: Key applications and Protocols ‖ Wiley Publications 2nd Edition

References:

1. Embedded Systems: Real-Time Interfacing to Arm(r) Cortex -M Microcontrollers: Volume-1 & 2 by Jonathan W Valvano
2. Designing the Internet of Things‖ by Adrian McEwen, Hakim Cassimally, Wiley Publications, 2012
3. . Embedded Real Time Systems: Concepts, Design and Programming by Dr. K.V.K.K.Prasad, DreamTech Publication, 2003.

E-Resources

1. http://www.itu.int/en/ITU-T/gsi/iot/Pages/default.aspx
2. http://electronicdesign.com/embedded/understanding-protocolsbehind-internet-things
3. http://eclipse.org/community/eclipse_newsletter/2014/february/articl e2.php
4. http://iot.eclipse.org/protocols.html
5. http://www.slideshare.net/paolopat/internet-ofthingsprotocolswar
6. http://www.slideshare.net/RealTimeInnovations/io-34485340
7. http://www.networkworld.com/article/2456421/internet-of-things/aguide-to-the confusing-internet-of-things-standards-world.html

Course Outcomes

After completion of the course, students will be able to:

1. Describe the fundamental concepts of IoT and its applications
2. Illustrate M2M concepts with protocols.
3. Develop applications using Python Scripting Language.
4. Build real world applications by applying Raspberry PI.
5. Examine web based services.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech. III Semester		
Code: A0623	**ARTIFICIAL INTELLIGENCE** (Open Elective)	**L**	**T**	**P**
Credits: 3		**3**	**-**	**-**

Prerequisites: Discrete Mathematics

Course objectives: This course enable the students to understand the basic fundamentals of Artificial Intelligence, determine various problem solving strategies, understand the logic concepts, different approaches to represent the knowledge, develop the expert systems in various phases and its applications, apply the fuzzy logic in various problem solving techniques

Module-I: Introduction **10 Periods**

Introduction to Artificial Intelligence: Introduction ,history, intelligent systems, foundations of AI, applications, tic-tac-tie game playing, development of AI languages, current trends in AI.

Module -II: Problem Solving **9 Periods**

Problem solving: state-space search and control strategies: Introduction, general problem solving, characteristics of problem, exhaustive searches, heuristic search techniques, iterative deepening a*, constraint satisfaction.
Problem reduction and game playing: Introduction, problem reduction, game playing, alphabeta pruning, two-player perfect information games.

Module -III: Logic Concepts and Knowledge Representation **10 Periods**

A: Logic Concepts - Introduction, propositional calculus, proportional logic, natural deduction system, axiomatic system, semantic tableau system in proportional logic, resolution refutation in proportional logic, predicate logic.
B: Knowledge Representation - Introduction, approaches to knowledge representation, knowledge representation using semantic network, extended semantic networks for KR, knowledge representation using frames advanced knowledge representation techniques: Introduction, conceptual dependency theory, script structure, cyc theory, case grammars, semantic web.

Module-IV: Expert System and Applications **10 Periods**

Introduction phases in building expert systems, expert system versus traditional systems, rule-based expert systems, blackboard systems truth maintenance systems, application of expert systems, list of shells and tools.

Module -V: Uncertainty Measure **9 Periods**

Probability theory: Introduction, Bayesian belief networks, certainty factor theory, dempster-shafer theory.

Fuzzy sets and fuzzy logic: Introduction, fuzzy sets, fuzzy set operations, types of membership functions, multi valued logic, fuzzy logic, linguistic variables and hedges, fuzzy propositions, inference rules for fuzzy propositions, fuzzy systems.

Text Books:

1. Saroj Kaushik, "**Artificial Intelligence**", CENGAGE Learning,
2. Stuart Russel, Peter Norvig, "**Artificial intelligence, A modern Approach**", 2nd ed, PEA
1. Rich, Kevin Knight, Shiv Shankar B Nair, "**Artificial Intelligence**", 3rd Ed, TMH
2. Patterson, **Introduction to Artificial Intelligence,** PHI

References:

1. George F Lugar, "**Artificial intelligence, structures and Strategies for Complex problem solving",** 5th edition, PEA
1. Ertel, Wolf Gang, "**Introduction to Artificial Intelligence",** Springer
2. Blay Whit BY, "**Artificial Intelligence**", Rosen Publishing.

E-Resources

1. https://i4iam.files.wordpress.com/2013/08/artificial-intelligence-by-rich-andknight.pdf
2. https://books.google.co.in/books?id=pVR9W5LEZUwC&printsec=frontcover&source=gbs_ge_summary_r&cad=0#v=onepage&q&f=false
3. https://www.journals.elsevier.com/artificial-intelligence/
4. http://www.ceser.in/ceserp/index.php/ijai
5. http://ndl.iitkgp.ac.in/document/yVCWqd6u7wgye1qwH9xY7_M07uyea_7zp_zRG3BvdUVy2TIab45fvPeNJfynQsAbmBEgDSUqzidwcse6xwotJA
6. http://ndl.iitkgp.ac.in/document/xttk-4kfhvUwVlXBW-YWRBg_vrHK12lgOzTVbb5oZ6eQOBjCWDfRvquHJLEOFENjI5AmOqRc9Ar3eJF4CGFrw

Course Outcomes

After completion of the course, students will be able to:

1. Describe the key components of the Artificial Intelligence field.
2. Identify various problem solving strategies.
3. Construct the solution for the problem using various logic and knowledge representation techniques.
4. Interpret the knowledge in various domains using expert systems.
5. Discover the solutions by using the probability theory and fuzzy logic.

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech III Sem		
Code: A41P1	TECHNICAL SEMINAR	L	T	P
Credits: 1		-	-	2

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech III Sem		
Code: A41P2	PROJECT / DISSERTATION PHASE - I	L	T	P
Credits: 8		-	-	16

2020-21 Onwards (MR-20)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	M.Tech IV Sem		
Code: A41P3	PROJECT / DISSERTATION PHASE - II	L	T	P
Credits: 16		-	-	32